Dynamic Failure Analysis

Static failure analysis is performed using an application board, probing or supplying dedicated signals using the EMMI/OBIRCH/LIT analysis tools. When a device fails during Latch-Up or in a dynamic mode MASER offers tools to perform semi dynamic failure localisation.

DYNAMIC FA AFTER LU

- Failure during LU test on MK2 tester
- Minimise LU failing mode on MK2
- Transfer the setup to LU bench setup
- LU bench setup
  - 4x power supply (software controlled)
  - SMU (software controlled)
- Fault localisation (EMMI/OBIRCH/LIT) using LU bench setup

DIGITAL PATTERN GENERATOR

- ByteParadigm
- 100 MHz operation
- Up to 32 MB memory buffer
- 16 bit digital pattern
- Optional external clocking
- Output voltage 1.25V to 3.3V
- USB-powered
- Win32/64 GUI
- C/C++ API programmable

SEMI DYNAMIC FA WITH D10

- Xcerra Diamond10 tester
- 2x DPIN96-32
- VIS-16
- DPS-16
- MultiWave
- DIBU
- Dedicated HW development for IC interface available

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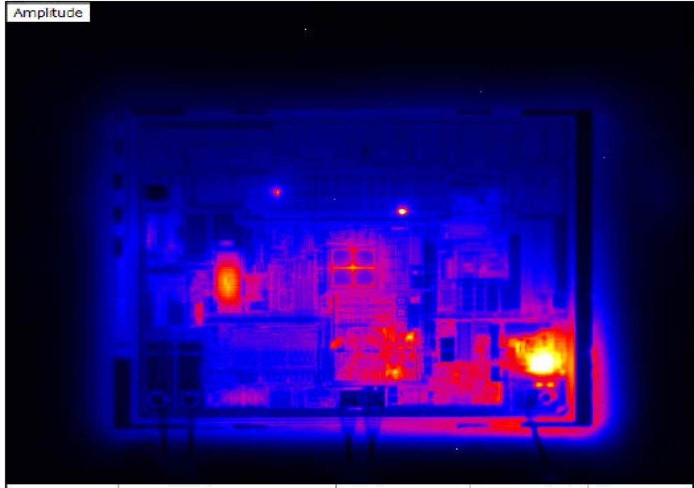
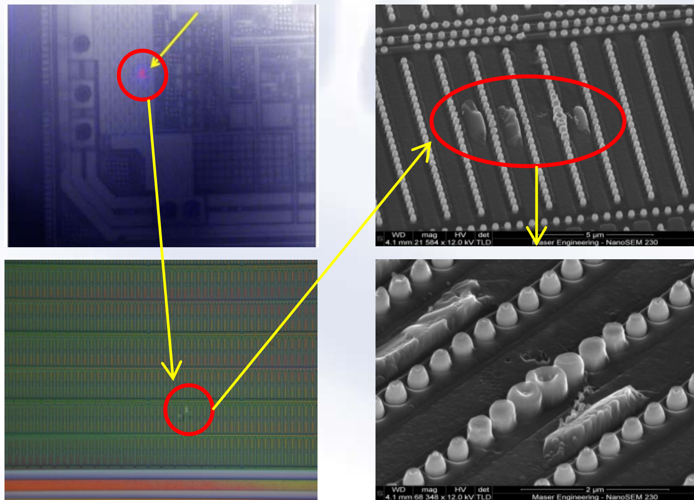
Dynamic Failure Analysis



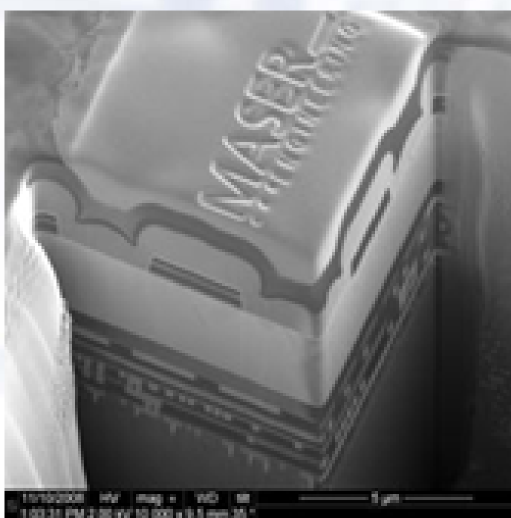
FAILURE LOCALISATION

- Front- and backside EMMI/OBIRCH analysis
- Package and silicon Lock-In Thermography (LIT) analysis
- EOTPR analysis on package level
- AFM analysis



FAILURE ANALYSIS

- FIB X-sectioning
- Delayering and SEM imaging
- (S)TEM sample preparation and imaging



SUMMARY

- Dynamic FA after LU
- Digital Pattern generator
- Semi Dynamic FA with D10
- Failure localisation
- Failure analysis

For more info please visit www.maser.nl
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